TITLE: MEMORY DEVICE HAVING TERMINALS FOR TRANSFERRING MULTIPLE TYPES OF DATA
INVENTOR: JOO CHOI
DOCKET NO.: 303.880US1

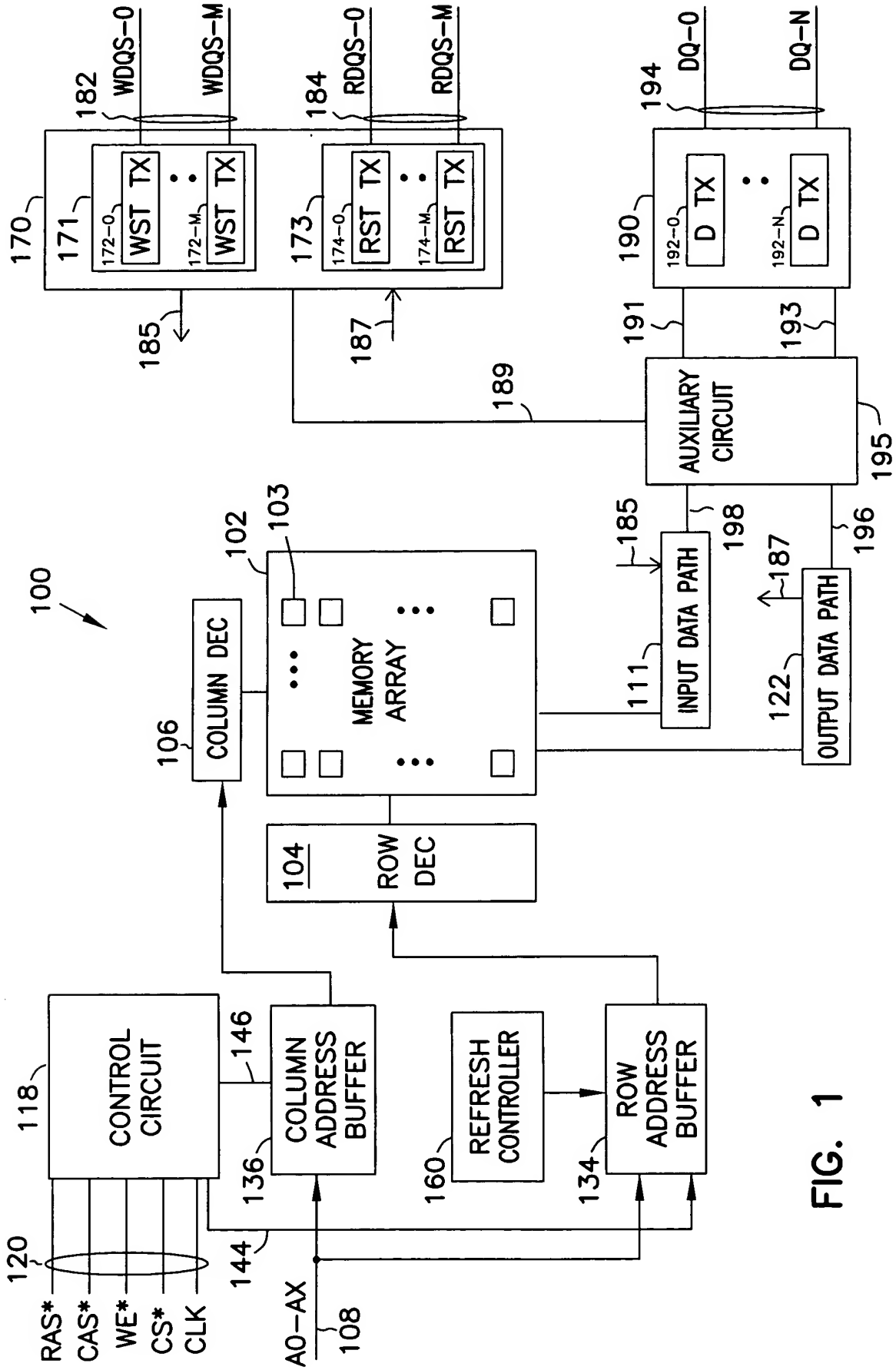

FIG. 1

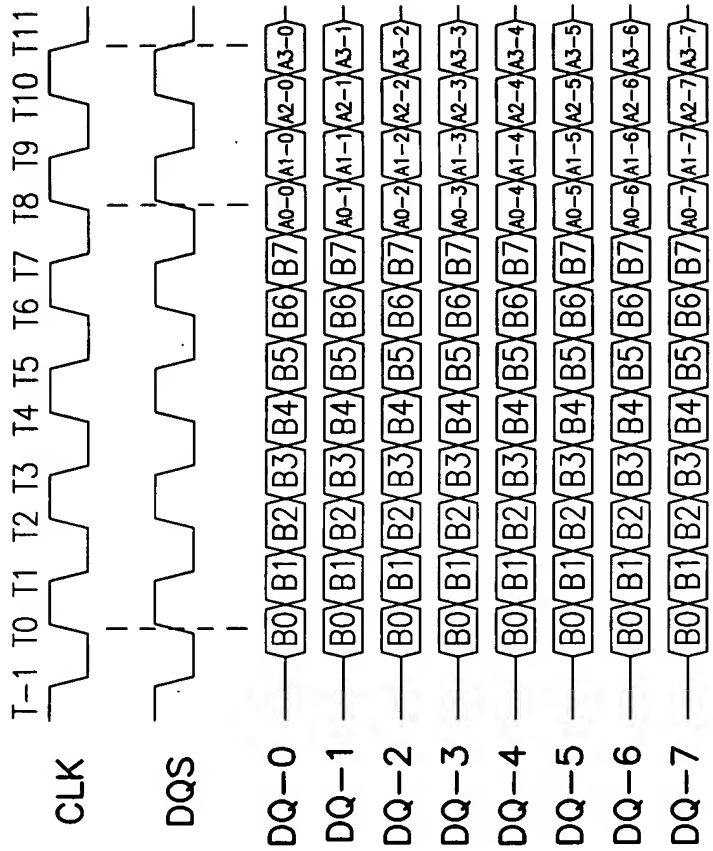
T-1 T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11
CLK
DQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
A0-0 A1-0 A2-0 A3-0
A0-1 A1-1 A2-1 A3-1
A0-2 A1-2 A2-2 A3-2
A0-3 A1-3 A2-3 A3-3
A0-4 A1-4 A2-4 A3-4
A0-5 A1-5 A2-5 A3-5
A0-6 A1-6 A2-6 A3-6
A0-7 A1-7 A2-7 A3-7

FIG. 2

TITLE: MEMORY DEVICE HAVING TERMINALS FOR TRANSFERRING MULTIPLE TYPES OF DATA
INVENTOR: JOO CHOI
DOCKET NO.: 303.880US1

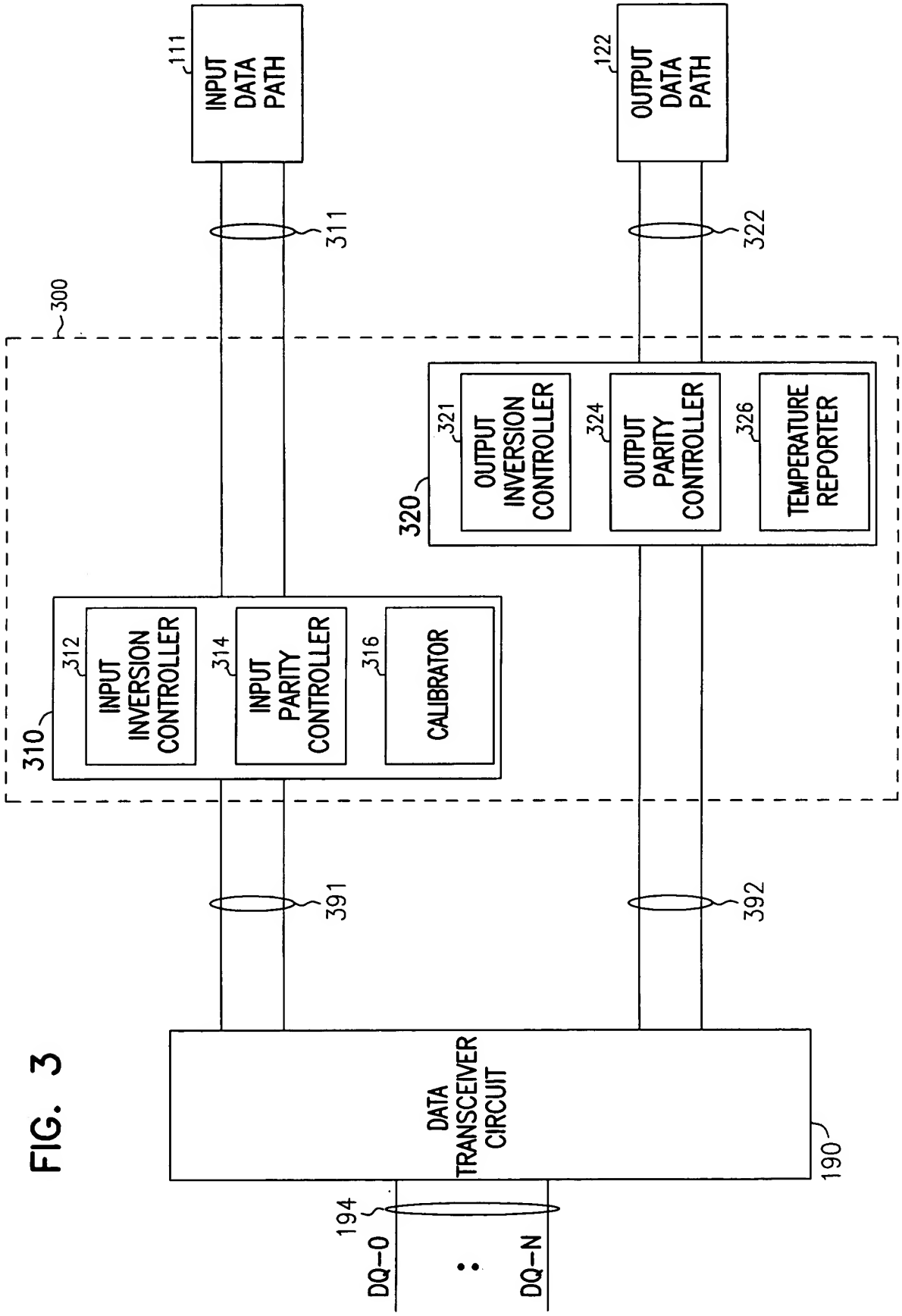

FIG. 3

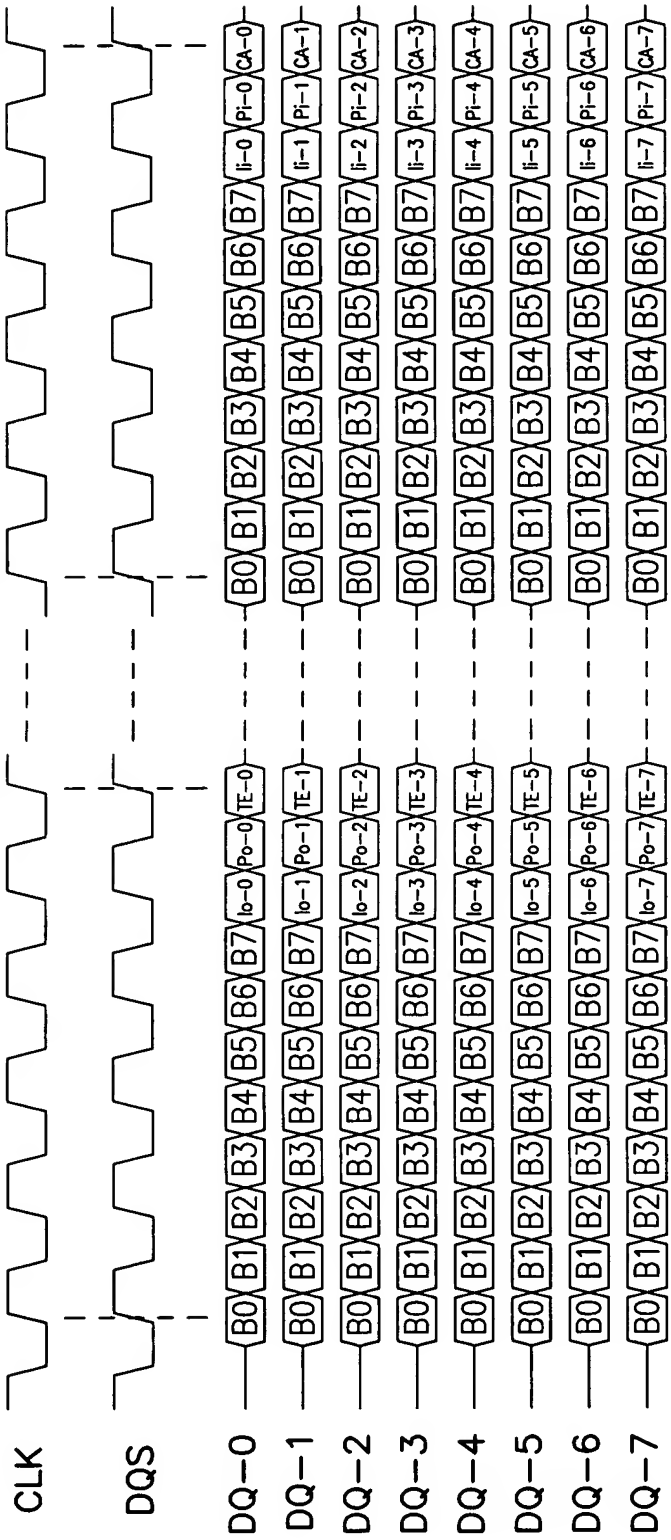
Ta
Tb
Tc
Td
CLK
DQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
Io-0 Po-0 TE-0
Ii-0 Pi-0 CA-0
Io-1 Po-1 TE-1
Ii-1 Pi-1 CA-1
Io-2 Po-2 TE-2
Ii-2 Pi-2 CA-2
Io-3 Po-3 TE-3
Ii-3 Pi-3 CA-3
Io-4 Po-4 TE-4
Ii-4 Pi-4 CA-4
Io-5 Po-5 TE-5
Ii-5 Pi-5 CA-5
Io-6 Po-6 TE-6
Ii-6 Pi-6 CA-6
Io-7 Po-7 TE-7
Ii-7 Pi-7 CA-7

FIG. 4

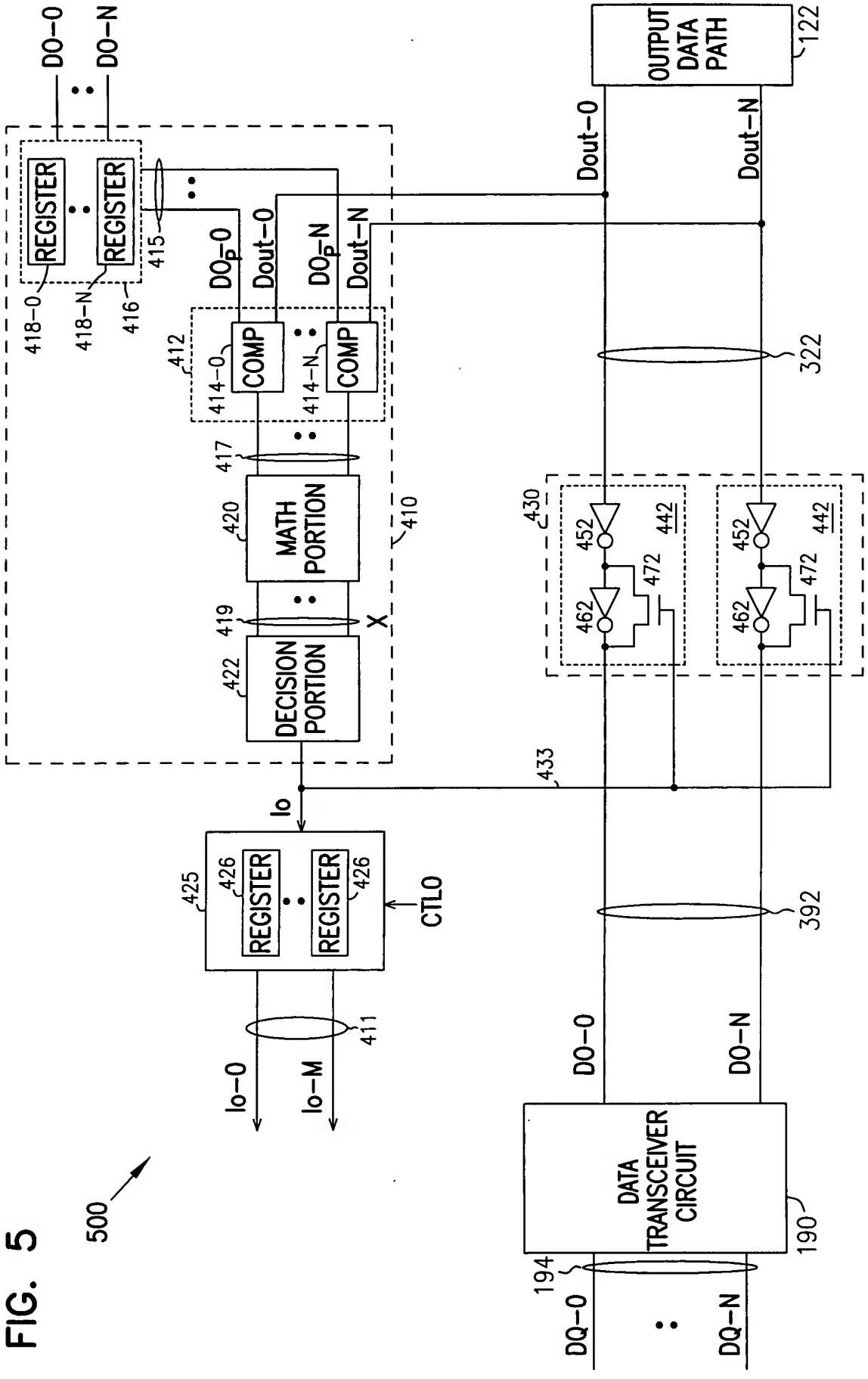
DO-0
DO-N
REGISTER
REGISTER
415
418-0
418-N
416
412
DOp-0
Dout-0
DOp-N
Dout-N
414-0
COMP
414-N
COMP
417
420
MATH PORTION
410
419
422
DECISION PORTION
X
Io
425
426
REGISTER
426
REGISTER
CTL0
411
Io-0
Io-M
500
OUTPUT DATA PATH
122
Dout-0
Dout-N
322
430
452
442
462
472
452
442
462
472
433
392
DO-0
DO-N
DATA TRANSCEIVER CIRCUIT
190
194
DQ-0
DQ-N

FIG. 5

	B0 B0 B0 B0 B0 B0 B0 B0			
DO_P	00000111	Io	X	Y
ROW 1 { Dout–0 TO Dout–7	11111000	1	8	
INVERTED (Dout–0 TO Dout–7)	00000111			0
	11110000	1	7	
	00001111			1
	11100000	1	6	
	00011111			2
	11000000	1	5	
	00111111			3
	10000000	0	4	
	01111111			4
ROW 6 { Dout–0 TO Dout–7	00000000	0	3	
INVERTED (Dout–0 TO Dout–7)	11111111			5
	00000001	0	2	
	11111110			6
	00000011	0	1	
	11111100			7
	00000111	0	0	
	11111000			8
	00001111	0	1	
	11110000			7
	00011111	0	2	
	11100000			6
	00111111	0	3	
	11000000			5
	01111111	0	4	
	10000000			4
	11111111	1	5	
	00000000			3
	11111110	1	6	
	00000001			2
ROW 16 { Dout–0 TO Dout–7	11111100	1	7	
INVERTED (Dout–0 TO Dout–7)	00000011			1

FIG. 6

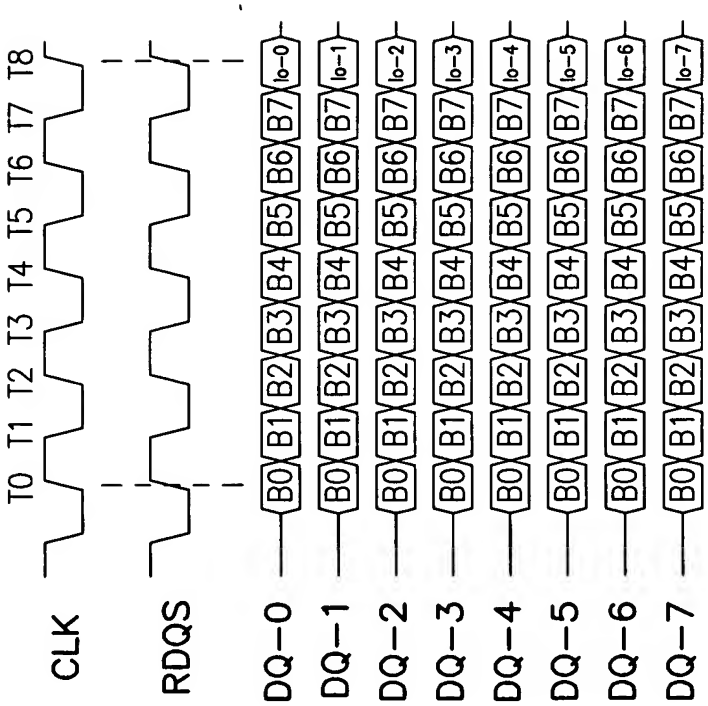
T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
RDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
Io-0
Io-1
Io-2
Io-3
Io-4
Io-5
Io-6
Io-7

FIG. 7

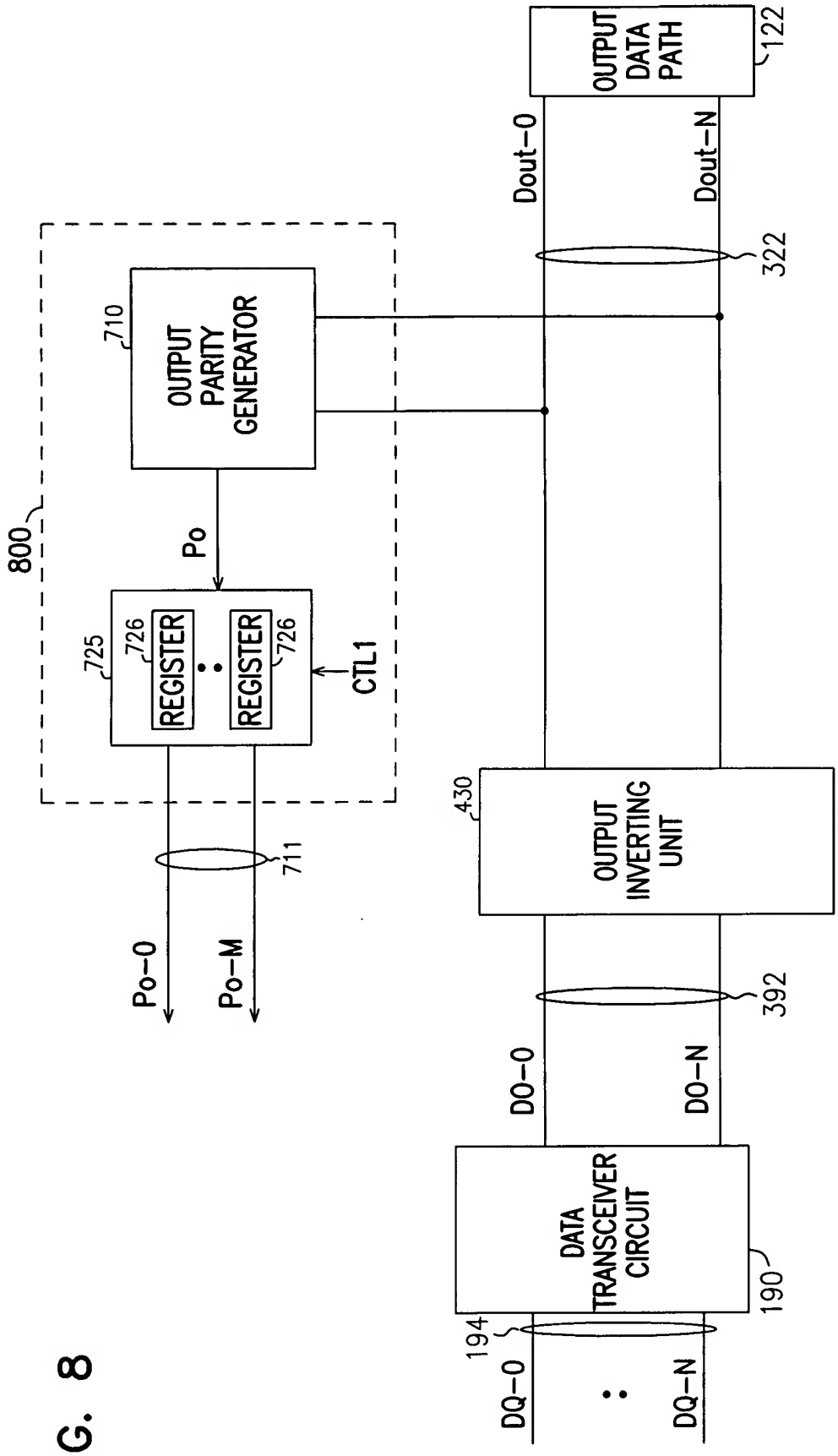
OUTPUT DATA PATH
122
Dout-0
Dout-N
322
800
710
OUTPUT PARITY GENERATOR
Po
725
726
REGISTER
REGISTER
726
CTL1
711
Po-0
Po-M
430
OUTPUT INVERTING UNIT
392
DO-0
DO-N
DATA TRANSCEIVER CIRCUIT
190
194
DQ-0
DQ-N

FIG. 8

	Dout-0 TO Dout-7 B0 B0 B0 B0 B0 B0 B0 B0	PO
ROW 1	00000000	0
	00000001	1
ROW 3	00000011	0
	00000111	1
	00001111	0
ROW 6	00011111	1
	00111111	0
	01111111	1
	11111111	0
	11111110	1
	11111100	0
	11111000	1
	11110000	0
ROW 14	11100000	1
	11000000	0
	10000000	1

FIG. 9

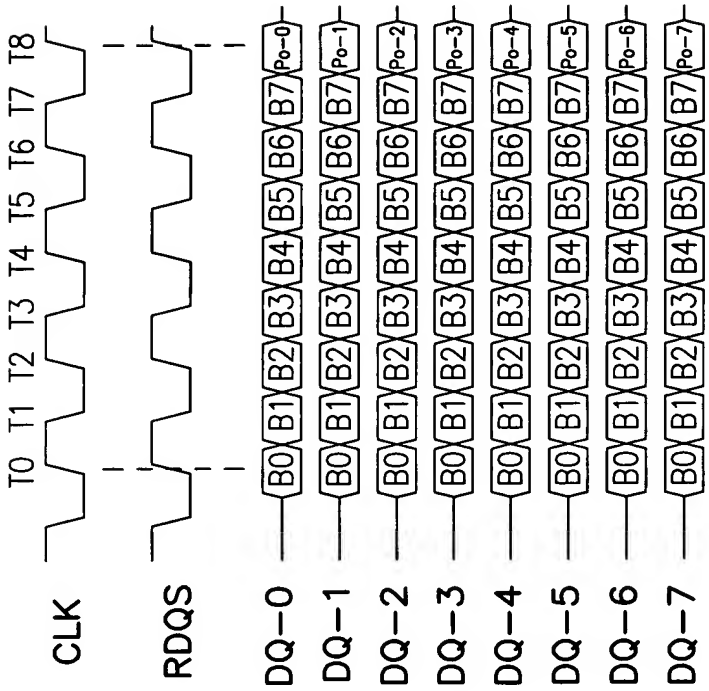
T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
RDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7 Po-0
B0 B1 B2 B3 B4 B5 B6 B7 Po-1
B0 B1 B2 B3 B4 B5 B6 B7 Po-2
B0 B1 B2 B3 B4 B5 B6 B7 Po-3
B0 B1 B2 B3 B4 B5 B6 B7 Po-4
B0 B1 B2 B3 B4 B5 B6 B7 Po-5
B0 B1 B2 B3 B4 B5 B6 B7 Po-6
B0 B1 B2 B3 B4 B5 B6 B7 Po-7

FIG. 10

TITLE: MEMORY DEVICE HAVING TERMINALS FOR TRANSFERRING MULTIPLE TYPES OF DATA
INVENTOR: JOO CHOI
DOCKET NO.: 303.880US1

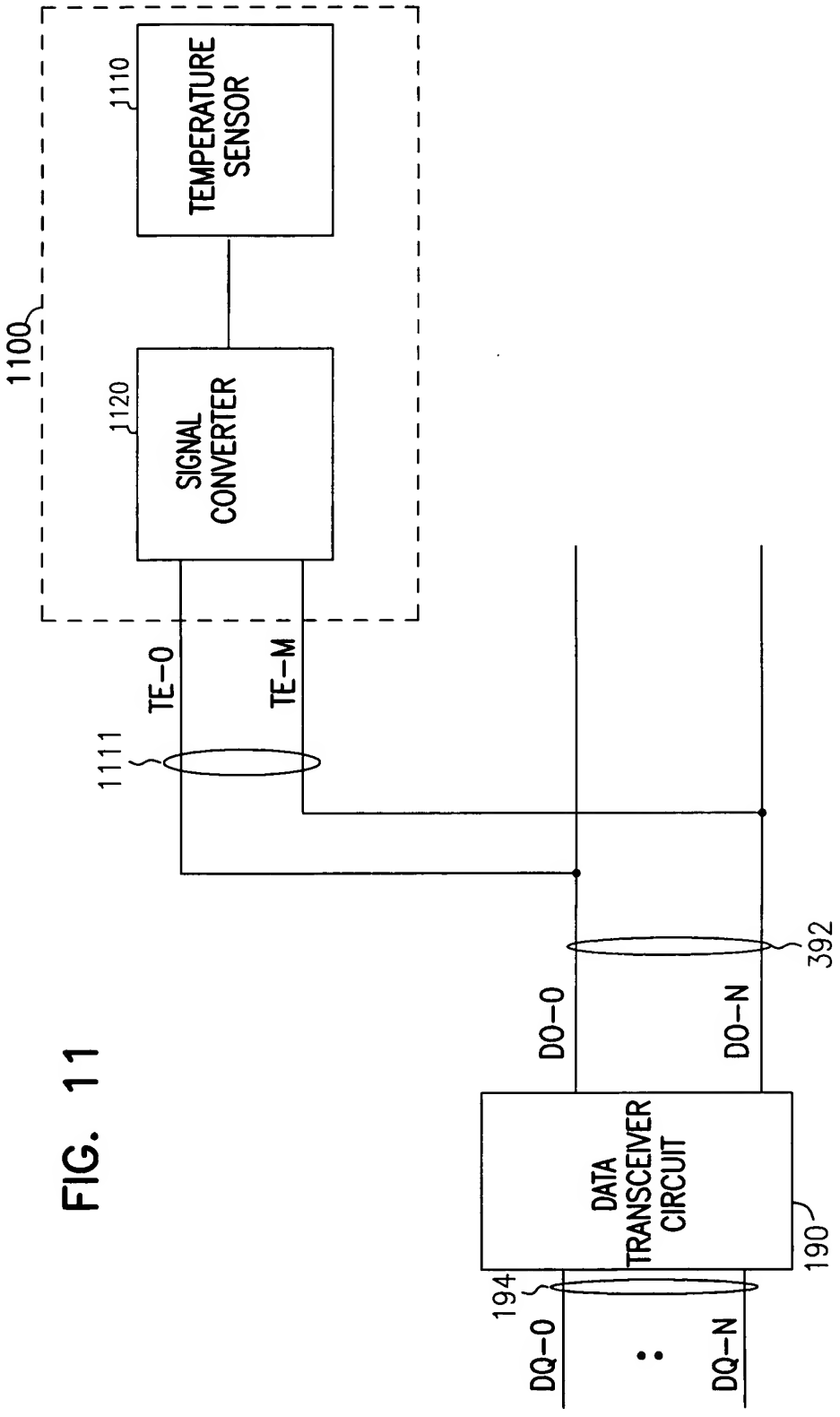

FIG. 11

BITS	TMP	TMP	TMP	TMP	TMP	TMP	TMP	TMP
TE-0	0	0	0	0	0	0	0	0
TE-1	0	0	0	0	0	0	0	1
TE-2	0	0	0	0	0	1	1	1
TE-3	0	0	0	0	1	1	1	1
TE-4	0	0	0	1	1	1	1	1
TE-5	0	0	0	1	1	1	1	1
TE-6	0	0	1	1	1	1	1	1
TE-7	0	1	1	1	1	1	1	1
TEMP °C	0	15	30	45	60	75	90	105

FIG. 12

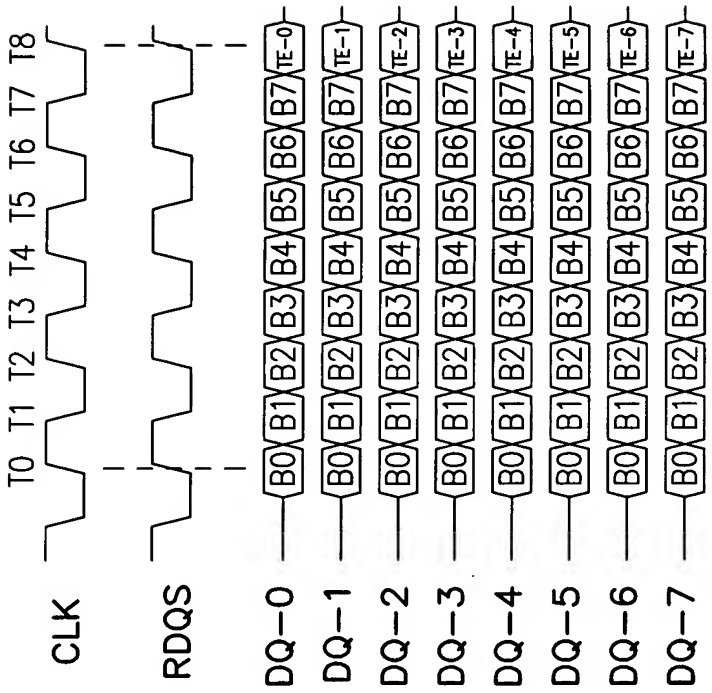
T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
RDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7 TE-0
B0 B1 B2 B3 B4 B5 B6 B7 TE-1
B0 B1 B2 B3 B4 B5 B6 B7 TE-2
B0 B1 B2 B3 B4 B5 B6 B7 TE-3
B0 B1 B2 B3 B4 B5 B6 B7 TE-4
B0 B1 B2 B3 B4 B5 B6 B7 TE-5
B0 B1 B2 B3 B4 B5 B6 B7 TE-6
B0 B1 B2 B3 B4 B5 B6 B7 TE-7

FIG. 13

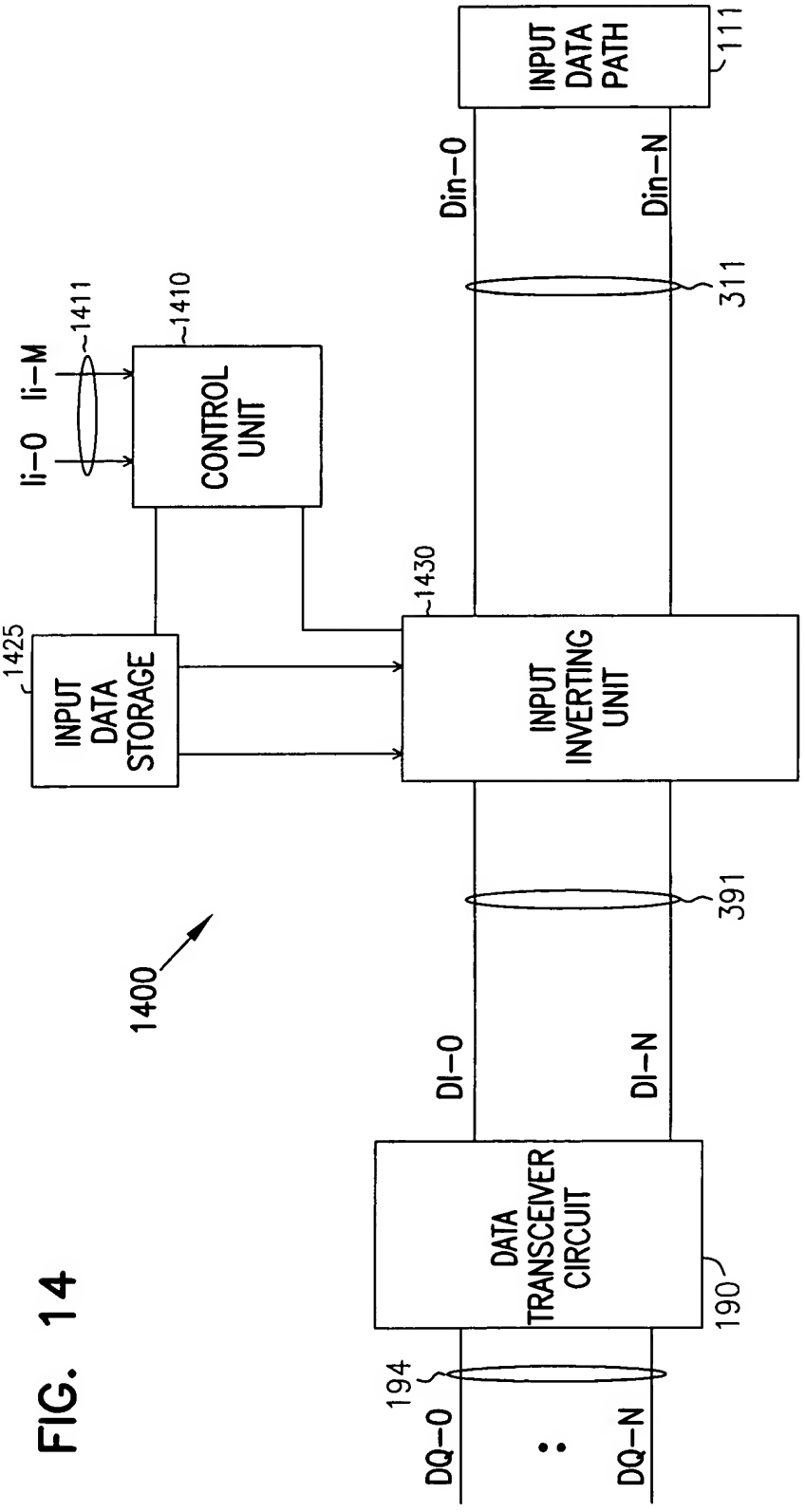
INPUT DATA PATH
111
Din-0
Din-N
311
CONTROL UNIT
1410
1411
Ii-0
Ii-M
1430
INPUT DATA STORAGE
1425
INPUT INVERTING UNIT
391
1400
DI-0
DI-N
DATA TRANSCEIVER CIRCUIT
190
194
DQ-0
DQ-N

FIG. 14

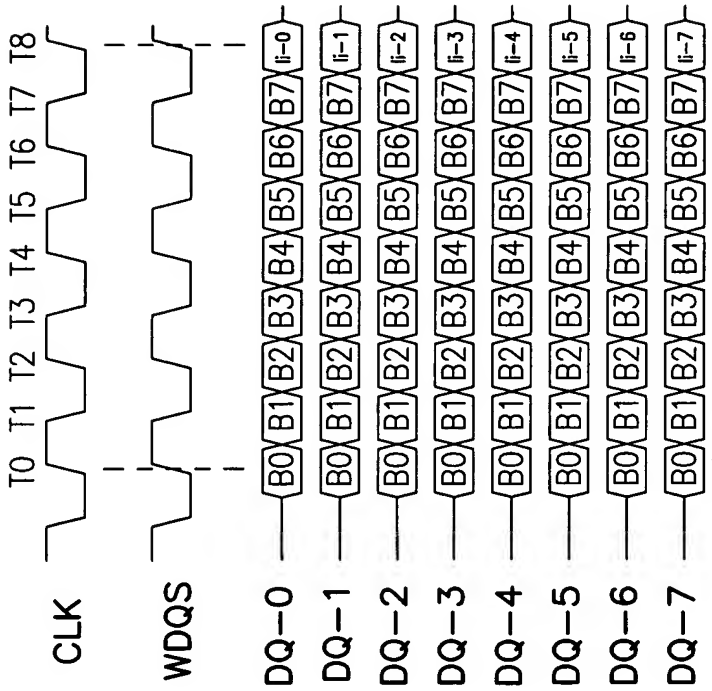
T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
WDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
i-0
i-1
i-2
i-3
i-4
i-5
i-6
i-7

FIG. 15

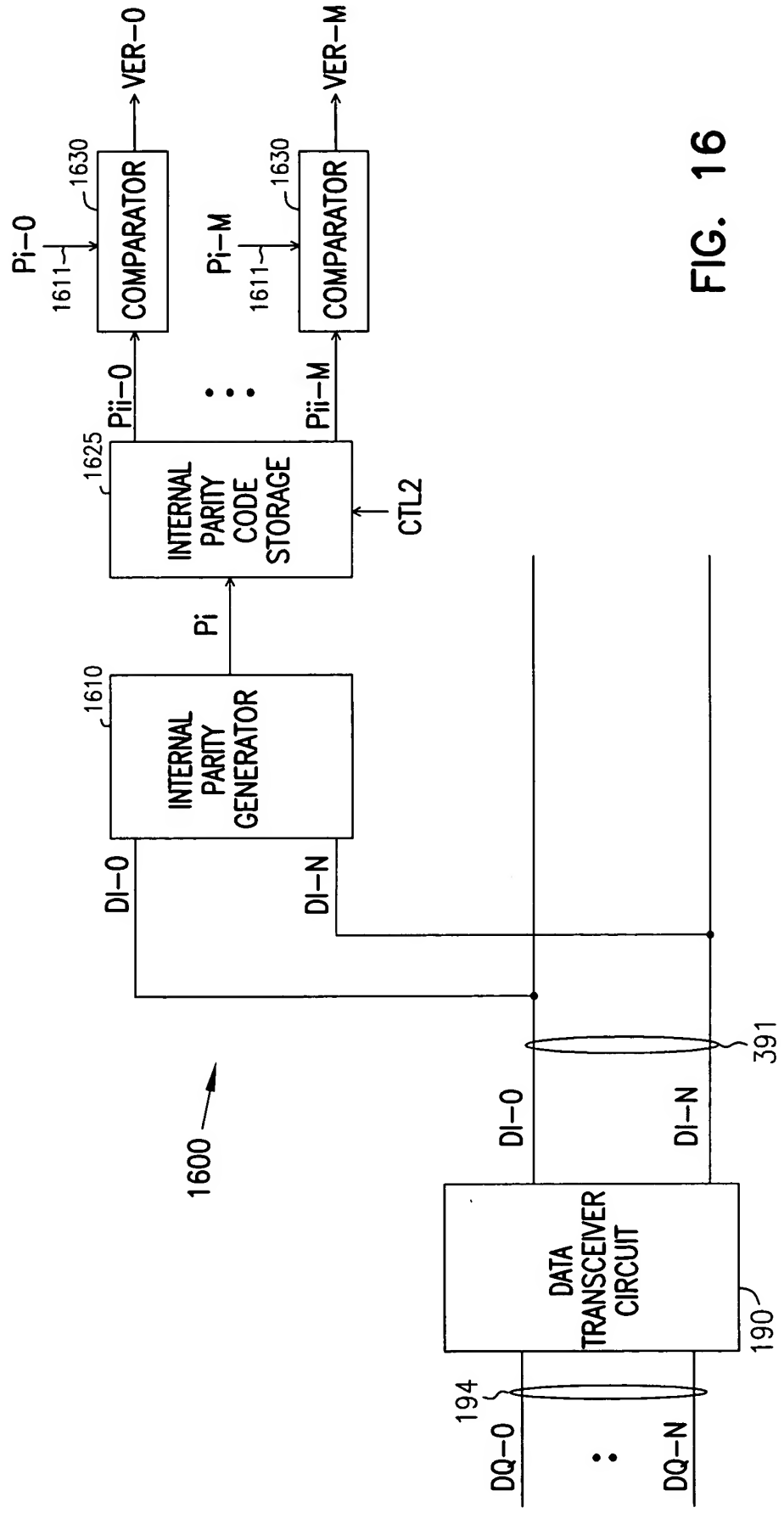
1600
DQ-0
DQ-N
194
DATA TRANSCEIVER CIRCUIT
190
DI-0
DI-N
391
DI-0
DI-N
INTERNAL PARITY GENERATOR
1610
Pi
INTERNAL PARITY CODE STORAGE
1625
CTL2
Pii-0
Pii-M
Pi-0
Pi-M
1611
COMPARATOR
1630
VER-0
VER-M

FIG. 16

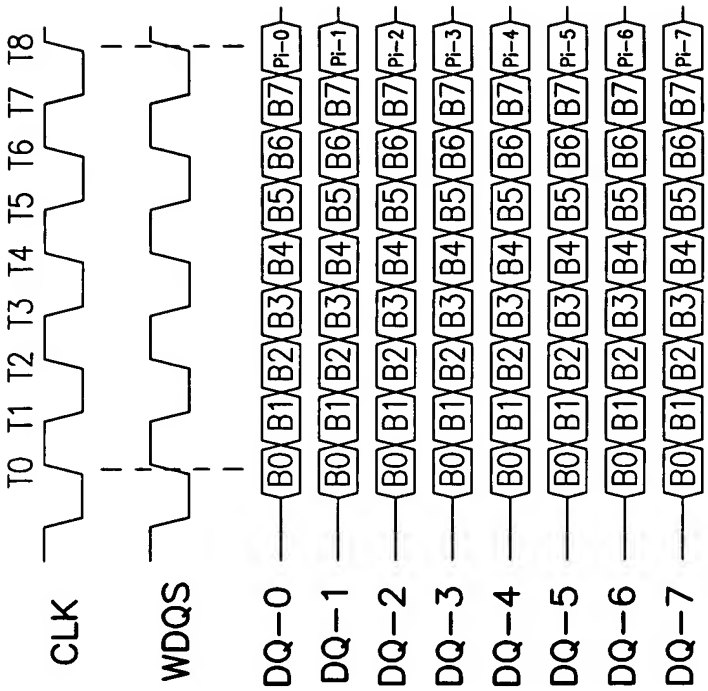
T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
WDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
Pi-0
Pi-1
Pi-2
Pi-3
Pi-4
Pi-5
Pi-6
Pi-7

FIG. 17

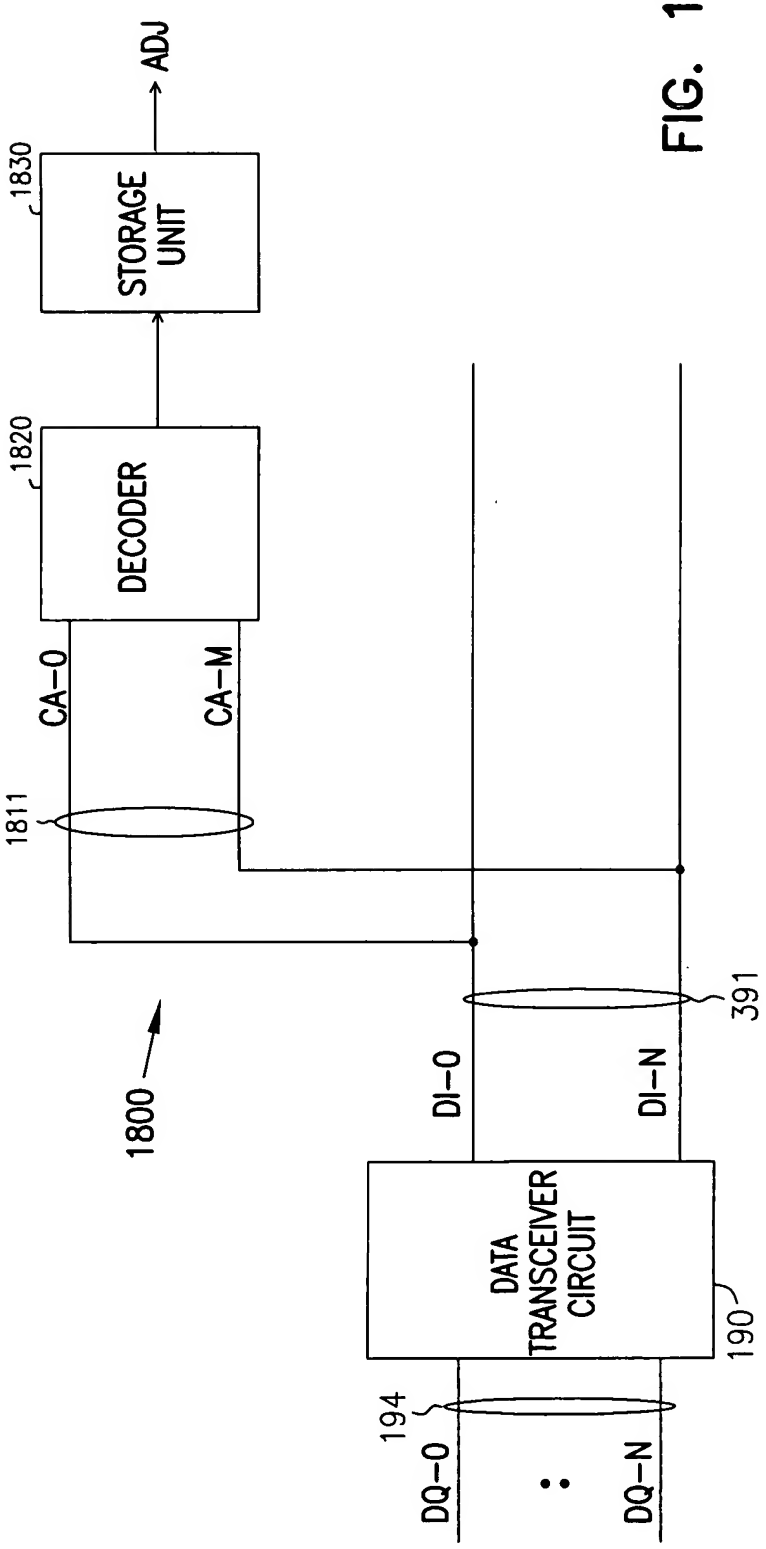
ADJ
1830
STORAGE UNIT
1820
DECODER
CA-0
CA-M
1811
1800
391
DI-0
DI-N
DATA TRANSCEIVER CIRCUIT
190
194
DQ-0
DQ-N

FIG. 18

BITS	CAL	CAL	CAL	CAL	CAL	CAL	CAL	CAL
CA–0	0	0	0	0	0	0	0	0
CA–1	0	0	0	0	0	0	0	1
CA–2	0	0	0	0	0	1	1	1
CA–3	0	0	0	0	1	1	1	1
CA–4	0	0	0	1	1	1	1	1
CA–5	0	0	0	1	1	1	1	1
CA–6	0	0	1	1	1	1	1	1
CA–7	0	1	1	1	1	1	1	1
DELAY	–200	–150	–100	–50	50	100	150	200

COL1 COL2 COL3 COL4 COL5 COL6 COL7 COL8

FIG. 19

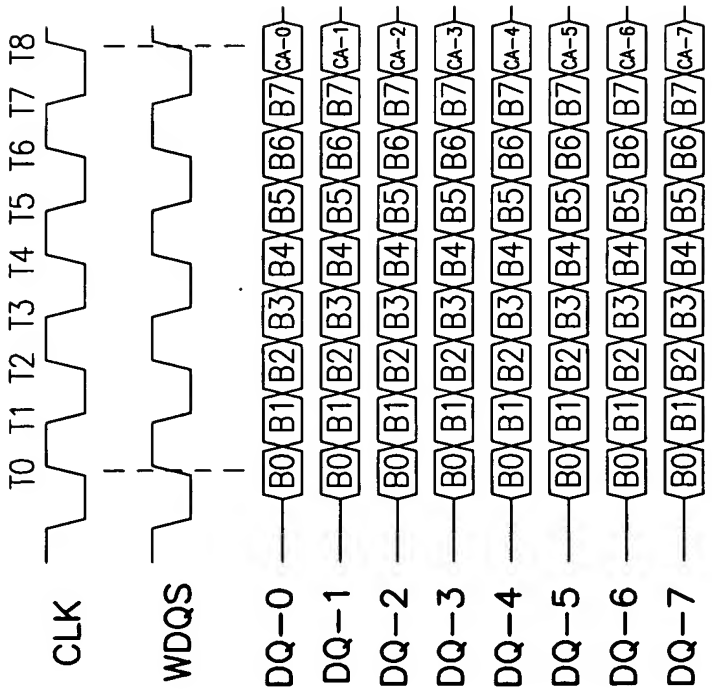
T0 T1 T2 T3 T4 T5 T6 T7 T8
CLK
WDQS
DQ-0
DQ-1
DQ-2
DQ-3
DQ-4
DQ-5
DQ-6
DQ-7
B0 B1 B2 B3 B4 B5 B6 B7
CA-0
CA-1
CA-2
CA-3
CA-4
CA-5
CA-6
CA-7

FIG. 20

TITLE: MEMORY DEVICE HAVING TERMINALS FOR TRANSFERRING MULTIPLE TYPES OF DATA
INVENTOR: JOO CHOI
DOCKET NO.: 303.880US1

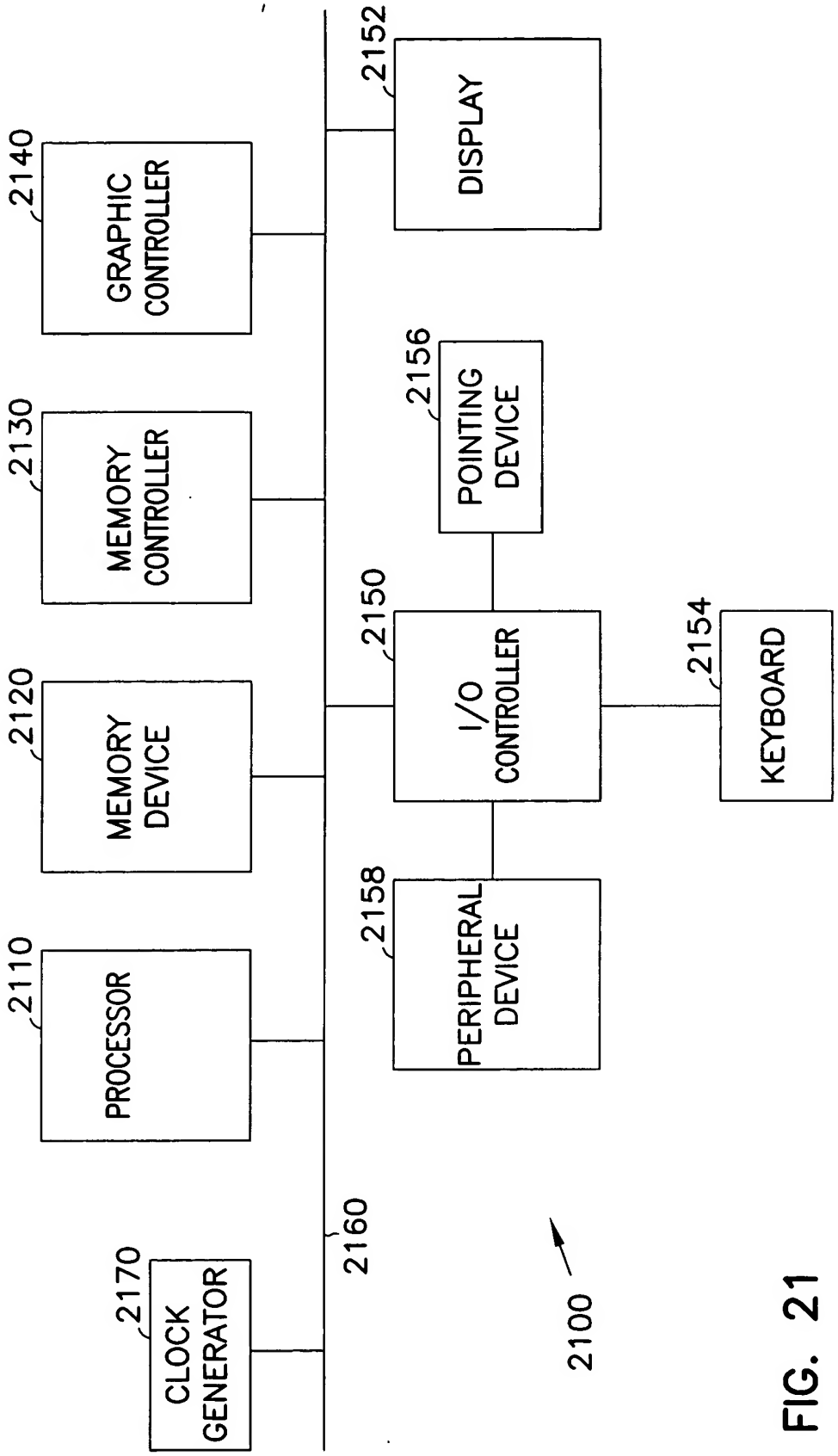

FIG. 21